WHAT IS CLAIMED IS:

1. A phase random access memory having a memory cell array arranged with a plurality of component areas, each of the component areas comprising:

a first conductive line extending in a first direction;

a plurality of second conductive lines extending in a second direction;

a phase-changeable film electrically connected to the first conductive line;

a first semiconductor region electrically connected to the phase-changeable film and defined within a first active region; and

a second semiconductor region defined within a second active region and separated from the first semiconductor region.

2. The phase random access memory of claim 1, wherein each of the component areas further comprises:

a first electrode connecting the first conductive line to the phase-changeable film;

a second electrode connecting the phase-changeable film to the first semiconductor region; and

a third electrode connecting the phase-changeable film to the second semiconductor region.

3. The phase random access memory of claim 1, wherein each of the

component areas further comprises a bitline contact through which the phase-changeable film electrically connects to the first conductive line, the bitline contact being shared by drain regions for each of a plurality of access transistors.

4. The phase random access memory of claim 1, wherein each of the component areas further comprises a plurality of third conductive lines extending in the second direction.

5. The phase random access memory of claim 4, wherein the plurality of third conductive lines are ground lines.

6. The phase random access memory of claim 1, wherein the first conductive line is a bitline and wherein each of the plurality of second conductive lines is a wordline.

7. A phase random access memory comprising:

a bitline;

a plurality of access transistors, each access transistor including a drain region; and

a phase-changeable film shared by the plurality access transistors.

8. The phase random access memory of claim 7, wherein the phase-changeable

film is connected to the bitline through a first electrode and connected to each respective drain region through at least one of a plurality of second electrodes.

9. The phase random access memory of claim 8, wherein the plurality of access transistors share the first electrode.

10. The phase random access memory of claim 7, wherein a source region of each access transistors is connected to a respective ground line.

11. The phase random access memory of claim 10, wherein the drain and source regions of each access transistor are defined within an active region.

12. The phase random access memory of claim 11, wherein the active region is divided into a plurality of regions isolated from each other.

13. The phase random access memory of claim 7, wherein a source region of each access transistor is commonly connected to a ground line.

14. The phase random access memory of claim 13, wherein the ground line is shared by the source region of each access transistor.

15. The phase random access memory of claim 7, wherein the plurality of

access transistors share a source region.

16. The phase random access memory of claim 7, wherein the phase-changeable film is connected to the bitline through a bitline contact shared by the drain region of each access transistor.

17. A phase random access memory having a memory cell array arranged with a plurality of component areas, each of the component areas comprising:

a first conductive line extending in a first direction;

a plurality of second conductive lines extending in a second direction;

a plurality of phase-changeable films electrically connected to the first conductive line; and

a semiconductor region electrically connected to the plurality of phase-changeable films, wherein at least one phase-changeable film of the plurality of phase changeable films is electrically connected to an adjacent semiconductor region of an adjacent component area.

18. The phase random access memory of claim 17, further comprising a plurality of bitline contacts through which the plurality of phase changeable films are connected to the semiconductor region, wherein at least one bitline contact of the plurality of bitline contacts connects the at least one phase-changeable film to the adjacent semiconductor region.

19. The phase random access memory of claim 17, further comprising a third conductive line, wherein at least one of third conductive line and the plurality of second conductive lines are twisted.

20. The phase random access memory of claim 19, wherein the first conductive line is a bitline, each of the plurality of second conductive lines is a wordline, and the third conductive line is a ground line.